PATENT ABSTRACTS OF JAPAN

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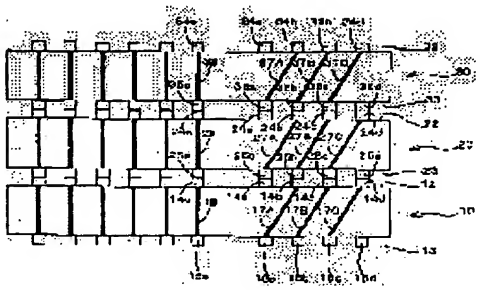
(54) THREE-DIMENSIONAL LAMINATED SEMICONDUCTOR DEVICE

(57)Abstract:
PROBLEM TO BE SOLVED: To provide a semiconductor device where signals can be applied to laminated semiconductor chips separately, even though these semiconductor chips have the same electrode structure.
SOLUTION: In the first semiconductor chip 10, salient electrodes 15a, 15b, 15c formed on a rear face 13 and salient electrodes 14b, 14c, 14d formed on a front face 12 are connected by oblique through electrodes 17A, 17B, 17C which obliquely cross both the rear and front faces of the chip. On the first semiconductor chip 10, a second and a third semiconductor chip 20, 30, each having the same electrode structure as the first one, are laminated. The first to third semiconductor chips 10, 20, 30 are connected to each other by the oblique through electrodes 17A, 17B, 17C, and so on and vertical through electrodes 18, 28, 38, and so on. The salient electrode 15a applies a signal to only the third semiconductor chip; the salient electrode 15b applies a signal to only the second semiconductor chip; and the salient electrode 15c applies a signal to only the first semiconductor chip.



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CLAIMS

[Claim(s)]
[Claim 1] It is the semiconductor device characterized by being the slanting penetration electrode with which at least one above-mentioned penetration electrode crosses aslant to the above-mentioned table rear face in the semiconductor device which has the penetration electrode penetrated at the front rear face.
[Claim 2] The semiconductor device characterized by having the perpendicular penetration electrode which intersects perpendicularly to the above-mentioned table rear face in a semiconductor device according to claim 1.
[Claim 3] The three-dimension laminating semiconductor device which carries out the two or more piece laminating of the semiconductor device according to claim 1 or 2, and is characterized by connecting the above-mentioned semiconductor device of each other electrically with the above-mentioned slanting penetration electrode at least.
[Claim 4] The three-dimension laminating semiconductor device which carries out the two or more piece laminating of the semiconductor device according to claim 2, and is characterized by connecting the above-mentioned semiconductor device of each other electrically with the above-mentioned slanting penetration electrode and a perpendicular penetration electrode.

[Translation done.]

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the three-dimension laminating semiconductor device which has the electrode penetrated at the front rear face and which comes to carry out the laminating of the LSI (large-scale integrated circuit), for example in the thickness direction.
[0002]
[Description of the Prior Art] Conventionally, as a three-dimension laminating semiconductor device, there is a thing as shown in drawing 3 . This three-dimension laminating semiconductor device carries out the laminating of the penetration electrodes 51A and 51B penetrated at the front rear face, the 1st which have ... 51 C, or the 3rd semiconductor chip 51, 52, and 53 in the thickness direction, and it is

formed in it. the above-mentioned penetration electrodes 51A and 51B -- in drawing 3 , it is mutually formed in the same longitudinal direction location about the above-mentioned semiconductor chips 51, 52, and 53 so that ... may intersect perpendicularly to the front rear face of semiconductor chips 51, 52, and 53 51 C. And penetration electrode [in the 1st thru/or the same longitudinal direction location of the 3rd semiconductor chip 51, 52, and 53]A [51] and 52A, 53A;51B, 52B, and 53B;51C, and 52C and 53C were connected, and the 1st thru/or the 3rd semiconductor chip 51, 52, and 53 of each other are connected electrically.

[0003]

[Problem(s) to be Solved by the Invention] However, the above-mentioned conventional three-dimension laminating semiconductor device the above-mentioned penetration electrodes 51A and 51B ... 51 C Since it is mutually formed in the same longitudinal direction location in semiconductor chips 51, 52, and 53 so that it may intersect perpendicularly to the front rear face of semiconductor chips 51, 52, and 53 and Since any penetration electrode of the penetration electrodes 51A, 51B, and 51C was connected to the 3rd semiconductor chip 53, there was a problem that the direct impression of the control signal etc. could not be carried out only at one semiconductor chips 51, 52, and 53, for example.

[0004] Then, in order to impress a signal only to one semiconductor chip in the semiconductor chip by which the laminating was carried out, the three-dimension laminating semiconductor device as shown in drawing 4 is proposed. This three-dimension laminating semiconductor device formed three penetration electrodes 55A, 55B, and 55C in the 1st semiconductor chip 55, formed two penetration electrodes 56A and 56B in the 2nd semiconductor chip 56, and has prepared one penetration electrode 57A in the 3rd semiconductor chip 57. And a signal is impressed to the 1st semiconductor chip 55 through penetration electrode 55C, and he impresses a signal to the 2nd semiconductor chip 56 through penetration electrode 55B and penetration electrode 56B, and is trying to impress a signal to the 3rd semiconductor chip 57 through penetration electrode 55A, penetration electrode 56A, and penetration electrode 57A.

[0005] However, since the above-mentioned three-dimension laminating semiconductor device needs to make the semiconductor chips 55, 56, and 57 with which it has a mutually different number of penetration electrodes, and penetration electrode structures differ, respectively, it has the problem that a production cost goes up sharply.

[0006] Then, as shown in drawing 5 , there is a three-dimension laminating semiconductor device it was made to impress a signal only to the 1st by which the laminating was carried out thru/or one semiconductor chip 61, 62, and 63 in the 3rd semiconductor chip 61, 62, and 63 using the semiconductor chips 61, 62, and 63 which have the same penetration electrode structure mutually. This three-dimension laminating semiconductor device prepares wiring 61e in the 1st semiconductor chip 61, prepares wiring 62e in the 2nd semiconductor chip 62, prepares wiring 63e in the 3rd semiconductor chip 63, and he is trying to impress a signal only to each semiconductor chip with the above-mentioned wiring 61e, 62e, and 63e.

[0007] However, the above-mentioned three-dimension laminating semiconductor device has the problem that the production yield falls and a production cost goes up, while the process for manufacturing the 1st thru/or the 3rd semiconductor chip 61, 62, and 63 becomes complicated, since a mutually different patterning process is needed for the 1st thru/or the 3rd semiconductor chip 61, 62, and 63 in order to give mutually different wiring 61e, 62e, and 63e.

[0008] Then, although the purpose of this invention has the penetration electrode of each other in the same location and has the same electrode structure, when the laminating of it is carried out and a three-dimension laminating semiconductor device is formed, it can impress a signal for every semiconductor device, and, moreover, structure is to offer an easy and cheap semiconductor device and the three-dimension laminating semiconductor device using it.

[0009]

[Means for Solving the Problem] In order to attain the above-mentioned purpose, in the semiconductor device which has the penetration electrode which penetrates the semiconductor device of this invention at the front rear face, at least one above-mentioned penetration electrode is characterized by being the slanting penetration electrode which crosses aslant to the above-mentioned table rear face.

[0010] Since the above-mentioned slanting penetration electrode crosses aslant to the front rear face of a semiconductor device according to the semiconductor device of this invention, this slanting penetration electrode connects the terminal of the location in which a front face differs from a rear face etc. Therefore, the terminal of the location in which the front face of a semiconductor device differs from a rear face etc. is connected, without taking about this semiconductor device separately like before, and preparing wiring of business.

[0011] The semiconductor device of 1 operation gestalt is characterized by having the perpendicular penetration electrode which intersects perpendicularly to the above-mentioned table rear face.

[0012] Since it also has the perpendicular penetration electrode which intersects perpendicularly to the front rear face of a semiconductor device while having the slanting penetration electrode which crosses aslant to the front rear face of a semiconductor device according to the semiconductor device of 1 operation gestalt, the above-mentioned slanting penetration electrode and a perpendicular penetration electrode connect the terminal of the same location and a different location etc. in the front face and rear face of the above-mentioned semiconductor device. Therefore, when this semiconductor device changes the arrangement location and the arrangement number of the above-mentioned slanting penetration electrode and a perpendicular penetration electrode, a connection pattern predetermined between the front face of a semiconductor device and rear faces is obtained.

[0013] The three-dimension laminating semiconductor device of this invention carries out the two or more piece laminating of the above-mentioned semiconductor device, and is characterized by connecting the above-mentioned semiconductor device of each other electrically with the above-mentioned slanting penetration electrode at least.

[0014] According to the three-dimension laminating semiconductor device of this invention, the above-mentioned slanting penetration electrode connects the location where the semiconductor devices by which the two or more piece laminating was carried out [above-mentioned] differ. Therefore, even if it carries out the two or more piece laminating of the semiconductor device which has a slanting penetration electrode or a perpendicular penetration electrode in the same location, and has the same electrode structure, the above-mentioned slanting penetration electrode connects only the predetermined semiconductor device of the two or more semiconductor devices by which the laminating was carried out without connecting all the two or more semiconductor devices by which the laminating was carried out. Consequently, the three-dimension laminating semiconductor device which can impress a signal only to a predetermined semiconductor device is obtained, without using the semiconductor device of different electrode structure, or wiring a semiconductor device further.

[0015] The three-dimension laminating semiconductor device of this invention carries out the two or more piece laminating of the above-mentioned semiconductor device, and is characterized by connecting the above-mentioned semiconductor device of each other electrically with the above-mentioned slanting penetration electrode and a perpendicular penetration electrode.

[0016] According to the three-dimension laminating semiconductor device of this invention, between the semiconductor devices which have a slanting penetration electrode and a perpendicular penetration electrode and by which the two or more piece laminating was carried out is connected with the above-mentioned slanting penetration electrode and a perpendicular penetration electrode. Therefore, while a perpendicular penetration electrode connects all the semiconductor devices by which the two or more piece laminating was carried out [above-mentioned], a slanting penetration electrode connects only either of the semiconductor devices by which the two or more piece laminating was carried out [above-mentioned]. Consequently, in spite of carrying out the laminating of the semiconductor device which has the same electrode structure, while impressing a signal to all semiconductor devices, the three-dimension laminating semiconductor device which can impress a signal only to a predetermined semiconductor device is obtained.

[0017]

[Embodiment of the Invention] Hereafter, the gestalt of implementation of illustration explains this invention to a detail.

[0018] Drawing 1 is the sectional view showing the semiconductor chip as a semiconductor device

concerning 1 operation gestalt of this invention. the projection electrodes 4a, 4b, 4c, 4d, and 4e with which this semiconductor chip 1 becomes a front face 2 from Au(gold) -- the projection electrodes 5a, 5b, 5c, 5d, and 5e which are equipped with ... and become a rear face 3 from Au -- it has ...

[0019] The projection electrodes 4b, 4c, and 4d of the above-mentioned front face 2 and the projection electrodes 5a, 5b, and 5c of a rear face 3 are electrically connected by the slanting penetration electrodes 7A, 7B, and 7C which consist of Cu (copper) which crosses aslant to the above-mentioned front face 2 and a rear face 3. More in detail, projection electrode 4c of a front face 2 and projection electrode 5b of a rear face 3 are connected by slanting penetration electrode 7B, and 4d of projection electrodes of a front face 2 and projection electrode 5c of a rear face 3 are connected for projection electrode 4b of a front face 2, and projection electrode 5a of a rear face 3 by slanting penetration electrode 7A by slanting penetration electrode 7C. That is, in the front rear faces 2 and 3 of a semiconductor chip 1, only one pitch shifted the electrode and the above-mentioned slanting penetration electrodes 7A, 7B, and 7C have connected.

[0020] On the other hand, projection electrode 4e of the front face 2 of a semiconductor chip 1 and projection electrode 5e of a rear face 3 are electrically connected by the perpendicular penetration electrode 8 which intersects perpendicularly to the front rear faces 2 and 3 of a semiconductor chip 1. As for the above-mentioned slanting penetration electrodes 7A, 7B, and 7C and the perpendicular penetration electrode 8, the peripheral surface is covered with the insulating semi-conductor oxide film.

[0021] The above-mentioned semiconductor chip 1 is the following, and is made and manufactured.

[0022] First, from the front-face 2 side of semi-conductor section 1a which has the thickness of 50 micrometers, the include angle of 21.8 degrees is made to the normal of this front face 2, and the laser beam of a minor diameter spot is irradiated by carbon dioxide laser or the YAG laser. Then, a through hole with a diameter of 10 micrometers which crosses aslant to the front rear faces 2 and 3 of semi-conductor section 1a is formed. A longitudinal direction is made to produce a 20-micrometer gap in drawing 1 with the inclination of the 21.8 above-mentioned degrees between surface 2 side edge of the above-mentioned through hole, and rear-face 3 side edge. Then, the thermal oxidation film is formed in the inside of the above-mentioned through hole, Cu plating is performed to the inside and the slanting penetration electrodes 7A, 7B, and 7C are formed. And with Au plating, the projection electrodes 4a, 4b, 4c, and 4d are set on the front face 2 of the above-mentioned semi-conductor section 1a, and spacing of 20 micrometers is formed in it. Moreover, the projection electrodes 5a, 5b, 5c, and 5d are formed in the rear face 3 of the above-mentioned semi-conductor section 1a projection electrodes [of the above-mentioned front face 2 / 4a 4b, 4c, and 4d] directly under. In here, the projection electrodes 4b, 4c, and 4d of the above-mentioned front face 2 and the projection electrodes 5a, 5b, and 5c of a rear face 3 are respectively connected by the above-mentioned slanting penetration electrodes 7A, 7B, and 7C.

[0023] Furthermore, from the front-face 2 side of the above-mentioned semi-conductor partial 1a, a right angle is made to the above-mentioned front face 2, the laser beam of a minor diameter spot is irradiated, and a through hole with a diameter of 10 micrometers which intersects perpendicularly to the front rear faces 2 and 3 of semi-conductor partial 1a is formed. The thermal oxidation film is formed in the inside of this through hole, Cu plating is performed to that inside and the perpendicular penetration electrode 8 is formed. The projection electrodes 4e and 5e are formed in the both ends of the above-mentioned perpendicular penetration electrode 8 of the front face 2 of the above-mentioned semi-conductor partial 1a, and a rear face 3 with Au plating, respectively.

[0024] Drawing 2 is the sectional view showing the three-dimension laminating semiconductor device in the operation gestalt of this invention, carries out the laminating of the semiconductor chips 10, 20, and 30 which have the same structure as the above-mentioned semiconductor chip 1 in the thickness direction, and is formed.

[0025] This three-dimension laminating semiconductor device has joined respectively the projection electrodes 14a, 14b, 14c, and 14d formed on the front face 12 of the 1st semiconductor chip 10 between the 1st semiconductor chip 10 and the 2nd semiconductor chip 20, and the projection electrodes 25a, 25b, 25c, and 25d formed in the front face 23 of the 2nd semiconductor chip 20 by the

solid phase diffusion welding of Au-Au. Moreover, the projection electrodes 24a, 24b, 24c, and 24d formed in the front face 22 of the 2nd semiconductor chip 20 and the projection electrodes 35a, 35b, 35c, and 35d formed in the rear face 33 of the 3rd semiconductor chip 30 are respectively joined by the solid phase diffusion welding of Au-Au. moreover, the projection electrodes 14e and 14e of the front face 12 of the 1st semiconductor chip 10 -- the projection electrodes 25e and 25e of the rear face 23 of ... and the 2nd semiconductor chip 20 ... and the projection electrodes 24e and 14e of the front face 22 of the 2nd semiconductor chip 20 -- the projection electrodes 35e and 53e of the rear face 33 of ... and the 3rd semiconductor chip 30 ... is respectively joined by the solid phase diffusion welding of Au-Au. In here, you may join using the approach of stiffening adhesives besides the solid phase diffusion welding of Au-Au where a pressure welding is only carried out, and obtaining a flow, and anisotropy electric conduction adhesives, and ordinary temperature junction may be used.

[0026] The projection electrodes 15a, 15b, and 15c of the rear face 13 of the 1st semiconductor chip 10 have connected this three-dimension laminating semiconductor device to the slanting penetration electrodes 17A and 17B and mutually different semiconductor chips 10, 20, and 30 through ..., respectively 17 C. That is, the above-mentioned projection electrode 15c has connected with 14d of projection electrodes of the front face 12 of the 1st semiconductor chip 10 through slanting penetration electrode 17C. the above-mentioned projection electrode 35b -- slanting penetration electrode 17B and slanting penetration electrode 27C -- minding -- half-- it has connected with 24d of projection electrodes of the front face 22 of a chip 20 the 2nd conductor. Furthermore, the above-mentioned projection electrode 15a has connected with 34d of projection electrodes of the front face 32 of the 3rd semiconductor chip 30 through slanting penetration electrode 17A, slanting penetration electrode 27B, and slanting penetration electrode 37C.

[0027] The selection signal line of the 2nd semiconductor chip 20 is connected with 24d of projection electrodes of the 2nd semiconductor chip 20, and the selection signal line of the 3rd semiconductor chip 30 is connected with 34d of projection electrodes of the 3rd semiconductor chip 30 for the selection signal line of the 1st semiconductor chip 10 at 14d of projection electrodes of the 1st semiconductor chip 10 of the above.

[0028] In the three-dimension laminating semiconductor device of the above-mentioned configuration, the logic signal of (1, 0, 0) is impressed to the projection terminals 15a, 15b, and 15c of the rear face 13 of the 1st semiconductor chip 10 of the above. If it does so, a signal will be impressed only to the 3rd semiconductor chip 30 connected to the above-mentioned projection terminal 15a, and the circuit formed in the 3rd semiconductor chip 30 will be in an active state. moreover -- and (0, 1, 0) to each logic signal of (0, 0, 1), the circuit formed in each of the 2nd semiconductor chip 20 and the 1st semiconductor chip 10, respectively will be in an active state exclusively, respectively.

[0029] on the other hand -- the projection terminals 15e and 15e of the front face 13 of the 1st semiconductor chip 10 -- if a signal is impressed to ..., a signal will be impressed to the 1st thru/or all the 3rd semiconductor chip 10, 20, and 30.

[0030] Thus, since the above-mentioned three-dimension laminating semiconductor device carries out the laminating of the semiconductor chips 10, 20, and 30 which have the same penetration electrode structure and can impress a signal to these semiconductor chips 10, 20, and 30 according to an individual, without carrying out the laminating of the semiconductor chips 55, 56, and 57 which have mutually different penetration electrode structure [as / in the conventional three-dimension laminating semiconductor device shown in drawing 4], it can reduce sharply the production cost of a three-dimension laminating semiconductor device.

[0031] Moreover, since it is not necessary to form the wiring 61e, 62e, and 63e for leading about of a pattern [as / in the conventional three-dimension laminating semiconductor device shown in drawing 5] which is mutually different in semiconductor chips 61, 62, and 63, a process can be simplified conventionally, while being able to improve the production yield, productive efficiency can be improved, consequently the production cost of a three-dimension laminating semiconductor device can be reduced.

[0032] Although it prepared three ... at a time in right-hand side in drawing 2 17 C, the three-dimension laminating semiconductor device of the above-mentioned operation gestalt of the slanting penetration

electrodes 17A and 17B and the location which arranges a slanting penetration electrode is good anywhere, and may arrange a slanting penetration electrode and a perpendicular penetration electrode by turns. Moreover, how many pieces are sufficient as the number of a slanting penetration electrode and a perpendicular penetration electrode, and all may be slanting penetration electrodes. Although all the penetration electrodes carried out the laminating of the semiconductor device which has the same electrode structure in the case of the slanting penetration electrode, the three-dimension laminating semiconductor device which can impress a signal to the semiconductor device by which the laminating was carried out according to an individual is obtained.

[0033] Although the three-dimension laminating semiconductor device of the above-mentioned operation gestalt carried out the three-piece laminating of the semiconductor chips 10, 20, and 30, two or more pieces [how many] are sufficient as the semiconductor device chip which carries out a laminating.

[0034]

[Effect of the Invention] As mentioned above, according to the semiconductor device of this invention, at least one penetration electrode can connect the terminal of the location in which the front face of a semiconductor device differs from a rear face etc. with the above-mentioned slanting penetration electrode, without preparing wiring [as / in the former] for leading about, since it is the slanting penetration electrode which crosses aslant to the front rear face of a semiconductor device so that clearly.

[0035] Since it has the perpendicular penetration electrode which intersects perpendicularly to the above-mentioned table rear face according to the semiconductor device of 1 operation gestalt and the above-mentioned slanting penetration electrode and a perpendicular penetration electrode connect the location where the front face and the rear face of the above-mentioned semiconductor device are the same, and a different location, a connection pattern predetermined between the front face of a semiconductor device and rear faces can obtain by changing the arrangement location and the arrangement number of the above-mentioned slanting penetration electrode and a perpendicular penetration electrode.

[0036] Since the three-dimension laminating semiconductor device of this invention carried out the two or more piece laminating of the above-mentioned semiconductor device and connected the above-mentioned semiconductor device of each other electrically with the above-mentioned slanting penetration electrode at least Since the above-mentioned slanting penetration electrode connects the predetermined semiconductor device of the two or more semiconductor devices even if it carries out the two or more piece laminating of the semiconductor device which has the same electrode structure The three-dimension laminating semiconductor device which can impress a signal only to the predetermined semiconductor device of the two or more semiconductor devices by which the laminating was carried out can be obtained without using the semiconductor device of different electrode structure, or wiring a semiconductor device further.

[0037] Since the three-dimension laminating semiconductor device of this invention carried out the two or more piece laminating of the above-mentioned semiconductor device and connected the above-mentioned semiconductor device of each other electrically with the above-mentioned slanting penetration electrode and the perpendicular penetration electrode, in spite of carrying out the laminating of the semiconductor device which has the same electrode structure, while impressing a signal to all semiconductor devices, the three-dimension laminating semiconductor device which can impress a signal only to a predetermined semiconductor device can be obtained.

[Translation done.]

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the sectional view showing the semiconductor device of the operation gestalt of this invention.
[Drawing 2] It is the sectional view showing the three-dimension laminating semiconductor device which carried out the three-piece laminating of the semiconductor device shown in drawing 1 , and formed it.
[Drawing 3] It is the sectional view showing the three-dimension laminating semiconductor device which carried out the laminating of the semiconductor device which has the same conventional electrode structure, and formed it.
[Drawing 4] It is the sectional view showing the three-dimension laminating semiconductor device which carried out the laminating of the semiconductor device which has the conventional mutually different electrode structure, and formed it.
[Drawing 5] While carrying out the laminating of the semiconductor device which has the same conventional electrode structure, it is the sectional view showing the three-dimension laminating semiconductor device which gave mutually different wiring.
[Description of Notations]
10 1st Semiconductor Chip
12 Front Face of 1st Semiconductor Chip
13 Rear Face of 1st Semiconductor Chip
14a, 14b, 14c, 14d, 14e Projection electrode of the front face of the 1st semiconductor chip
15a, 15b, 15c, 15d, 15e Projection electrode of the rear face of the 1st semiconductor chip
17A, 17B, 17C Slanting penetration electrode of the 1st semiconductor chip
18 Perpendicular Penetration Electrode of 1st Semiconductor Chip
20 2nd Semiconductor Chip
24a, 24b, 24c, 24d, 24e Projection electrode of the front face of the 2nd semiconductor chip
25a, 25b, 25c, 25d, 25e Projection electrode of the rear face of the 2nd semiconductor chip
27A, 27B, 27C Slanting penetration electrode of the 2nd semiconductor chip
28 Perpendicular Penetration Electrode of 2nd Semiconductor Chip
30 3rd Semiconductor Chip
34a, 34b, 34c, 34d, 34e Projection electrode of the front face of the 3rd semiconductor chip
35a, 35b, 35c, 35d, 35e Projection electrode of the rear face of the 3rd semiconductor chip
37A, 37B, 37C Slanting penetration electrode of the 3rd semiconductor chip
38 Perpendicular Penetration Electrode of 3rd Semiconductor Chip

[Translation done.]

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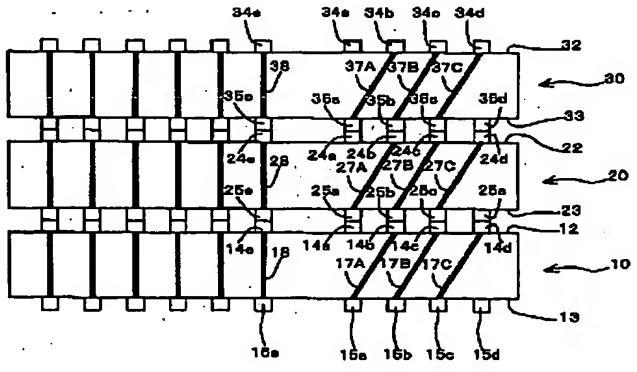
(54)【発明の名称】　３次元積層半導体装置

(57)【要約】
【課題】　同一の電極構造を有するにも拘わらず、積層された場合に半導体装置毎に信号を印加できる半導体装置を提供すること。
【解決手段】　第１半導体チップ１０は、裏面１３の突起電極１５ａ，１５ｂ，１５ｃと、表面１２の突起電極１４ｂ，１４ｃ，１４ｄとが、半導体チップ１０の表裏面に対して斜めに交差する斜め貫通電極１７Ａ，１７Ｂ，１７Ｃによって接続されていて、第１半導体チップ１０の上に、同一の電極構造を有する第２，第３半導体チップ２０，３０が積層されている。第１乃至第３半導体チップ１０，２０，３０は、斜め貫通電極１７Ａ，１７Ｂ，１７Ｃ・・・および垂直貫通電極１８，２８，３８・・・によって互いに接続されている。突起電極１５ａは第３半導体チップのみに、突起電極１５ｂは第２半導体チップのみに、突起電極１５ｃは第１半導体チップのみに、信号を印加する。



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【特許請求の範囲】

【請求項１】　表裏面に貫通する貫通電極を有する半導体装置において、

少なくとも１つの上記貫通電極は、上記表裏面に対して斜めに交差する斜め貫通電極であることを特徴とする半導体装置。

【請求項２】　請求項１に記載の半導体装置において、上記表裏面に対して直交する垂直貫通電極を有することを特徴とする半導体装置。

【請求項３】　請求項１または２に記載の半導体装置を２個以上積層して、少なくとも上記斜め貫通電極によって上記半導体装置を互いに電気的に接続したことを特徴とする３次元積層半導体装置。

【請求項４】　請求項２に記載の半導体装置を２個以上積層して、上記斜め貫通電極および垂直貫通電極によって、上記半導体装置を互いに電気的に接続したことを特徴とする３次元積層半導体装置。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】本発明は、表裏面に貫通する電極を有する例えばＬＳＩ（大規模集積回路）を、厚み方向に積層してなる３次元積層半導体装置に関する。

【０００２】

【従来の技術】従来、３次元積層半導体装置としては、図３に示すようなものがある。この３次元積層半導体装置は、表裏面に貫通する貫通電極５１Ａ，５１Ｂ，５１Ｃ・・・を有する第１乃至第３半導体チップ５１，５２，５３を、厚み方向に積層して形成されている。上記貫通電極５１Ａ，５１Ｂ，５１Ｃ・・・は、半導体チップ５１，５２，５３の表裏面に対して直交するように、かつ上記半導体チップ５１，５２，５３に関して、図３において互いに同じ横方向位置に形成されている。そして、第１乃至第３半導体チップ５１，５２，５３の同じ横方向位置にある貫通電極５１Ａ，５２Ａ，５３Ａ；５１Ｂ，５２Ｂ，５３Ｂ；５１Ｃ，５２Ｃ，５３Ｃを接続して、第１乃至第３半導体チップ５１，５２，５３を互いに電気的に接続している。

【０００３】

【発明が解決しようとする課題】しかしながら、上記従来の３次元積層半導体装置は、上記貫通電極５１Ａ，５１Ｂ，５１Ｃ・・・は、半導体チップ５１，５２，５３の表裏面に対して直交するように、かつ半導体チップ５１，５２，５３において互いに同じ横方向位置に形成されているので、貫通電極５１Ａ，５１Ｂ，５１Ｃのいずれの貫通電極も第３半導体チップ５３に接続しているから、例えばコントロール信号などを１つの半導体チップ５１，５２，５３のみに直接印加できないという問題があった。

【０００４】そこで、積層された半導体チップのうちの１つの半導体チップのみに信号を印加するために、図４

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に示すような３次元積層半導体装置が提案されている。この３次元積層半導体装置は、第１の半導体チップ５５に３個の貫通電極５５Ａ，５５Ｂ，５５Ｃを設け、第２半導体チップ５６に２個の貫通電極５６Ａ，５６Ｂを設け、第３半導体チップ５７に１個の貫通電極５７Ａを設けている。そして、貫通電極５５Ｃを介して第１半導体チップ５５に信号を印加して、貫通電極５５Ｂと、貫通電極５６Ｂとを介して第２半導体チップ５６に信号を印加して、貫通電極５５Ａと、貫通電極５６Ａと、貫通電極５７Ａとを介して第３半導体チップ５７に信号を印加するようにしている。

【０００５】しかしながら、上記３次元積層半導体装置は、互いに異なる数の貫通電極を有して貫通電極構造が異なる半導体チップ５５，５６，５７を夫々作る必要があるので、生産コストが大幅に上昇するという問題がある。

【０００６】そこで、図５に示すように、互いに同じ貫通電極構造を有する半導体チップ６１，６２，６３を用いて、積層された第１乃至第３半導体チップ６１，６２，６３のうちの１つの半導体チップ６１，６２，６３のみに信号を印加するようにした３次元積層半導体装置がある。この３次元積層半導体装置は、第１半導体チップ６１に配線６１ｅを設け、第２半導体チップ６２に配線６２ｅを設け、第３半導体チップ６３に配線６３ｅを設けて、上記配線６１ｅ，６２ｅ，６３ｅによって、各々の半導体チップのみに信号を印加するようにしている。

【０００７】しかしながら、上記３次元積層半導体装置は、第１乃至第３半導体チップ６１，６２，６３に、互いに異なる配線６１ｅ，６２ｅ，６３ｅを施すために、互いに異なるパターニング工程が必要になるので、第１乃至第３半導体チップ６１，６２，６３を製造するための工程が煩雑になると同時に、生産歩留りが低下して生産コストが上昇するという問題がある。

【０００８】そこで、本発明の目的は、互いに同じ位置に貫通電極を有して同一の電極構造を有するにも拘わらず、積層されて３次元積層半導体装置を形成した場合に半導体装置毎に信号を印加でき、しかも構造が簡単で安価な半導体装置と、それを用いた３次元積層半導体装置を提供することにある。

【０００９】

【課題を解決するための手段】上記目的を達成するため、本発明の半導体装置は、表裏面に貫通する貫通電極を有する半導体装置において、少なくとも１つの上記貫通電極は、上記表裏面に対して斜めに交差する斜め貫通電極であることを特徴としている。

【００１０】本発明の半導体装置によれば、上記斜め貫通電極が半導体装置の表裏面に対して斜めに交差しているので、この斜め貫通電極は、表面と裏面とで異なる位置の例えば端子などを接続する。したがって、この半導体装置は、従来のように別個に引き回し用の配線を設け

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ることなく、半導体装置の表面と裏面とで異なる位置の例えば端子などが接続される。

【００１１】１実施形態の半導体装置は、上記表裏面に対して直交する垂直貫通電極を有することを特徴としている。

【００１２】１実施形態の半導体装置によれば、半導体装置の表裏面に対して斜めに交差する斜め貫通電極を有すると共に、半導体装置の表裏面に対して直交する垂直貫通電極も有するので、上記斜め貫通電極と垂直貫通電極とが、上記半導体装置の表面と裏面とにおいて、同じ位置と異なる位置の例えば端子などを接続する。したがって、この半導体装置は、上記斜め貫通電極と垂直貫通電極の配置位置および配置個数を変えることによって、半導体装置の表面と裏面との間で所定の接続パターンが得られる。

【００１３】本発明の3次元積層半導体装置は、上記半導体装置を２個以上積層して、少なくとも上記斜め貫通電極によって上記半導体装置を互いに電気的に接続したことを特徴としている。

【００１４】本発明の3次元積層半導体装置によれば、上記斜め貫通電極が上記２個以上積層された半導体装置の異なる位置を接続する。したがって、同じ位置に斜め貫通電極または垂直貫通電極を有して同じ電極構造を有する半導体装置を２個以上積層しても、上記斜め貫通電極は、積層された２個以上の半導体装置の全てを接続しないで、積層された２個以上の半導体装置のうちの所定の半導体装置のみを接続する。その結果、異なる電極構造の半導体装置を用いたり、半導体装置にさらに配線を施すことなく、所定の半導体装置のみに信号を印加できる３次元積層半導体装置が得られる。

【００１５】本発明の３次元積層半導体装置は、上記半導体装置を２個以上積層して、上記斜め貫通電極および垂直貫通電極によって、上記半導体装置を互いに電気的に接続したことを特徴としている。

【００１６】本発明の３次元積層半導体装置によれば、上記斜め貫通電極および垂直貫通電極によって、斜め貫通電極および垂直貫通電極を有する２個以上積層された半導体装置の間を接続する。したがって、垂直貫通電極が上記２個以上積層された半導体装置の全てを接続する一方、斜め貫通電極が上記２個以上積層された半導体装置のうちのいずれかのみを接続する。その結果、同一の電極構造を有する半導体装置を積層するにも拘らず、全ての半導体装置に信号を印加する一方、所定の半導体装置のみにも信号を印加できる３次元積層半導体装置が得られる。

【００１７】

【発明の実施の形態】以下、本発明を図示の実施の形態により詳細に説明する。

【００１８】図１は、本発明の一実施形態に係る半導体装置としての半導体チップを示す断面図である。この半

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導体チップ１は、表面２にＡｕ（金）からなる突起電極４ａ，４ｂ，４ｃ，４ｄ，４ｅ・・・を備え、裏面３にＡｕからなる突起電極５ａ，５ｂ，５ｃ，５ｄ，５ｅ・・・を備える。

【００１９】上記表面２の突起電極４ｂ，４ｃ，４ｄと、裏面３の突起電極５ａ，５ｂ，５ｃは、上記表面２および裏面３に対して斜めに交差するＣｕ（銅）からなる斜め貫通電極７Ａ，７Ｂ，７Ｃによって電気的に接続されている。より詳しくは、表面２の突起電極４ｂと裏面３の突起電極５ａとが斜め貫通電極７Ａによって、表面２の突起電極４ｃと裏面３の突起電極５ｂとが斜め貫通電極７Ｂによって、表面２の突起電極４ｄと裏面３の突起電極５ｃとが斜め貫通電極７Ｃによって接続されている。すなわち、上記斜め貫通電極７Ａ，７Ｂ，７Ｃは、半導体チップ１の表裏面２，３において、電極を１ピッチだけシフトして接続している。

【００２０】一方、半導体チップ１の表面２の突起電極４ｅと、裏面３の突起電極５ｅは、半導体チップ１の表裏面２，３に対して直交する垂直貫通電極８によって電気的に接続されている。上記斜め貫通電極７Ａ，７Ｂ，７Ｃと垂直貫通電極８は、周面が絶縁性半導体酸化皮膜で覆われている。

【００２１】上記半導体チップ１は、以下のようにして製造する。

【００２２】まず、５０μｍの厚みを有する半導体部１ａの表面２側から、この表面２の法線に対して２１．８度の角度をなして、炭酸ガスレーザーもしくはＹＡＧレーザーによって小径スポットのレーザ光を照射する。そうして、半導体部１ａの表裏面２，３に対して斜めに交差する直径１０μｍの貫通穴を形成する。上記２１．８度の傾きによって、上記貫通穴の表面２側端と裏面３側端との間に、図１において横方向に２０μｍのずれを生じさせる。その後、上記貫通穴の内面に熱酸化膜を形成し、その内側にＣｕめっきを施して斜め貫通電極７Ａ，７Ｂ，７Ｃを形成する。そして、上記半導体部１ａの表面２に、Ａｕめっきによって突起電極４ａ，４ｂ，４ｃ，４ｄを２０μｍの間隔をおいて形成する。また、上記半導体部１ａの裏面３に、上記表面２の突起電極４ａ，４ｂ，４ｃ，４ｄの直下に、突起電極５ａ，５ｂ，５ｃ，５ｄを形成する。ここにおいて、上記表面２の突起電極４ｂ，４ｃ，４ｄと、裏面３の突起電極５ａ，５ｂ，５ｃとが、上記斜め貫通電極７Ａ，７Ｂ，７Ｃによって各々接続されるようにする。

【００２３】さらに、上記半導体部分１ａの表面２側から、上記表面２に対して直角をなして小径スポットのレーザ光を照射して、半導体部分１ａの表裏面２，３に対して直交する直径１０μｍの貫通穴を形成する。この貫通穴の内面に熱酸化膜を形成し、その内側にＣｕめっきを施して、垂直貫通電極８を形成する。上記半導体部分１ａの表面２および裏面３の上記垂直貫通電極８の両端

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部に、Ａｕめっきによって夫々突起電極４ｅ，５ｅを形成する。

【００２４】図２は、本発明の実施形態における３次元積層半導体装置を示す断面図であり、上記半導体チップ１と同一の構造を有する半導体チップ１０，２０，３０を厚み方向に積層して形成されている。

【００２５】この３次元積層半導体装置は、第１半導体チップ１０と第２半導体チップ２０との間において、第１半導体チップ１０の表面１２に形成された突起電極１４ａ，１４ｂ，１４ｃ，１４ｄと、第２半導体チップ２０の表面２３に形成された突起電極２５ａ，２５ｂ，２５ｃ，２５ｄとを、Ａｕ－Ａｕの固相拡散接合によって各々接合している。また、第２半導体チップ２０の表面２２に形成された突起電極２４ａ，２４ｂ，２４ｃ，２４ｄと、第３半導体チップ３０の裏面３３に形成された突起電極３５ａ，３５ｂ，３５ｃ，３５ｄとを、Ａｕ－Ａｕの固相拡散接合によって各々接合している。また、第１半導体チップ１０の表面１２の突起電極１４ｅ，１４ｅ・・・と第２半導体チップ２０の裏面２３の突起電極２５ｅ，２５ｅ・・・と、かつ、第２半導体チップ２０の表面２２の突起電極２４ｅ，１４ｅ・・・と第３半導体チップ３０の裏面３３の突起電極３５ｅ，５３ｅ・・・とを、Ａｕ－Ａｕの固相拡散接合によって各々接合している。ここにおいて、Ａｕ－Ａｕの固相拡散接合の他に、単に圧接した状態で接着剤を硬化させて導通を得る方法や、異方性導電接着剤を用いて接合してもよく、常温接合を用いてもよい。

【００２６】この３次元積層半導体装置は、第１半導体チップ１０の裏面１３の突起電極１５ａ，１５ｂ，１５ｃが、斜め貫通電極１７Ａ，１７Ｂ，１７Ｃ・・・を介して、互いに異なる半導体チップ１０，２０，３０に夫々接続している。すなわち、上記突起電極１５ｃが、斜め貫通電極１７Ｃを介して、第１半導体チップ１０の表面１２の突起電極１４ｄに接続している。上記突起電極３５ｂは、斜め貫通電極１７Ｂと斜め貫通電極２７Ｃとを介して、半第２導体チップ２０の表面２２の突起電極２４ｄに接続している。さらに、斜め貫通電極１７Ａと斜め貫通電極２７Ｂと斜め貫通電極３７Ｃとを介して、上記突起電極１５ａが、第３半導体チップ３０の表面３２の突起電極３４ｄに接続しでいる。

【００２７】上記第１半導体チップ１０の突起電極１４ｄには第１半導体チップ１０のセレクト信号線を、第2半導体チップ２０の突起電極２４ｄには第２半導体チップ２０のセレクト信号線を、第3半導体チップ３０の突起電極３４ｄには第３半導体チップ３０のセレクト信号線を連結している。

【００２８】上記構成の３次元積層半導体装置において、上記第１半導体チップ１０の裏面１３の突起端子１５ａ，１５ｂ，１５ｃに、（１，０，０）の論理信号を印加する。そうすると、上記突起端子１５ａに接続された第３半導体チップ３０のみに信号が印加されて、第３半導体チップ３０に形成された回路が能動状態になる。また、（０，１，０）および、（０，０，１）の各論理信号に対しては、夫々第２半導体チップ２０および、第１半導体チップ１０の各々に形成された回路が夫々排他的に能動状態になる。

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【００２９】一方、第１半導体チップ１０の表面１３の突起端子１５ｅ，１５ｅ・・・に信号を印加すると、第１乃至第３半導体チップ１０，２０，３０の全てに信号が印加される。

【００３０】このように、上記３次元積層半導体装置は、図４に示した従来の３次元積層半導体装置におけるような互いに異なる貫通電極構造を有する半導体チップ５５，５６，５７を積層することなく、同一の貫通電極構造を有する半導体チップ１０，２０，３０を積層して、この半導体チップ１０，２０，３０に個別に信号を印加できるので、３次元積層半導体装置の生産コストを大幅に削減することができる。

【００３１】また、図５に示した従来の３次元積層半導体装置におけるように、半導体チップ６１，６２，６３に、互いに異なるパターンの引き回し用配線６１ｅ，６２ｅ，６３ｅを形成する必要がないため、従来よりも工程を簡素化できて、生産歩留りを向上できると共に生産効率を向上でき、その結果、３次元積層半導体装置の生産コストを低減できる。

【００３２】上記実施形態の３次元積層半導体装置は、斜め貫通電極１７Ａ，１７Ｂ，１７Ｃ・・・を図２において右側に３個づつ設けたが、斜め貫通電極を配置する位置はどこでもよく、また、斜め貫通電極と垂直貫通電極とを交互に配置してもよい。また、斜め貫通電極および垂直貫通電極の個数は何個でもよく、全てが斜め貫通電極であってもよい。全ての貫通電極が斜め貫通電極の場合、同一の電極構造を有する半導体装置を積層したにも拘らず、積層された半導体装置に個別に信号を印加できる3次元積層半導体装置が得られる。

【００３３】上記実施形態の３次元積層半導体装置は、半導体チップ１０，２０，３０を３個積層したが、積層する半導体装置チップは２個以上の何個でもよい。

【００３４】

【発明の効果】以上より明らかなように、本発明の半導体装置によれば、少なくとも１つの貫通電極が、半導体装置の表裏面に対して斜めに交差する斜め貫通電極であるので、従来におけるような引き回し用の配線を設けることなく、上記斜め貫通電極によって、半導体装置の表面と裏面とで異なる位置の例えば端子などを接続できる。

【００３５】１実施形態の半導体装置によれば、上記表裏面に対して直交する垂直貫通電極を有するので、上記斜め貫通電極と垂直貫通電極とが上記半導体装置の表面と裏面の同じ位置と異なる位置を接続するから、上記斜

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め貫通電極と垂直貫通電極の配置位置および配置個数を変えることによって、半導体装置の表面と裏面との間で所定の接続パターンを得ることができる。

【００３６】本発明の3次元積層半導体装置は、上記半導体装置を２個以上積層して、少なくとも上記斜め貫通電極によって上記半導体装置を互いに電気的に接続したので、同じ電極構造を有する半導体装置を２個以上積層しても、上記斜め貫通電極が２個以上の半導体装置のうちの所定の半導体装置を接続するから、異なる電極構造の半導体装置を用いたり、半導体装置にさらに配線を施すことなく、積層された２個以上の半導体装置のうちの所定の半導体装置のみに信号を印加できる３次元積層半導体装置を得ることができる。

【００３７】本発明の３次元積層半導体装置は、上記半導体装置を２個以上積層して、上記斜め貫通電極および垂直貫通電極によって、上記半導体装置を互いに電気的に接続したので、同一の電極構造を有する半導体装置を積層するにも拘らず、全ての半導体装置に信号を印加する一方、所定の半導体装置のみにも信号を印加できる３次元積層半導体装置を得ることができる。

【図面の簡単な説明】

【図１】　この発明の実施形態の半導体装置を示す断面図である。

【図２】　図１に示した半導体装置を３個積層して形成した３次元積層半導体装置を示す断面図である。

【図３】　従来の同一の電極構造を有する半導体装置を積層して形成した３次元積層半導体装置を示す断面図である。

【図４】　従来の互いに異なる電極構造を有する半導体装置を積層して形成した３次元積層半導体装置を示す断面図である。

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【図５】　従来の、同一の電極構造を有する半導体装置を積層すると共に、互いに異なる配線を施した３次元積層半導体装置を示す断面図である。

【符号の説明】

１０　第１半導体チップ

１２　第１半導体チップの表面

１３　第１半導体チップの裏面

１４ａ，１４ｂ，１４ｃ，１４ｄ，１４ｅ　第１半導体チップの表面の突起電極

１５ａ，１５ｂ，１５ｃ，１５ｄ，１５ｅ　第１半導体チップの裏面の突起電極

１７Ａ，１７Ｂ，１７Ｃ　第１半導体チップの斜め貫通電極

１８　第１半導体チップの垂直貫通電極

２０　第２半導体チップ

２４ａ，２４ｂ，２４ｃ，２４ｄ，２４ｅ　第２半導体チップの表面の突起電極

２５ａ，２５ｂ，２５ｃ，２５ｄ，２５ｅ　第２半導体チップの裏面の突起電極

２７Ａ，２７Ｂ，２７Ｃ　第２半導体チップの斜め貫通電極

２８　第２半導体チップの垂直貫通電極

３０　第３半導体チップ

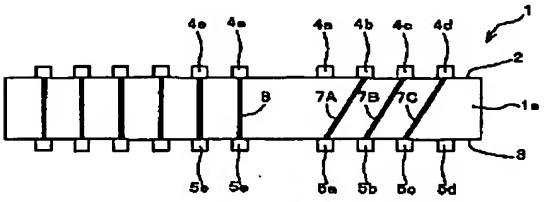
３４ａ，３４ｂ，３４ｃ，３４ｄ，３４ｅ　第３半導体チップの表面の突起電極

３５ａ，３５ｂ，３５ｃ，３５ｄ，３５ｅ　第３半導体チップの裏面の突起電極

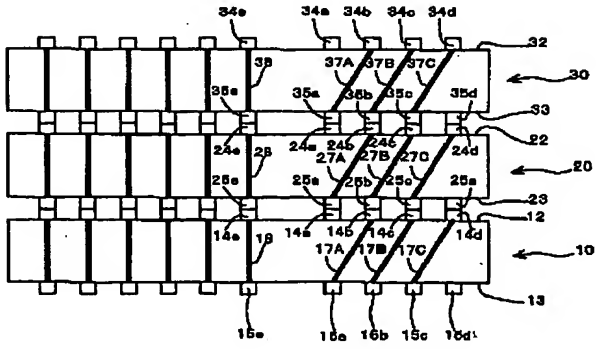
３７Ａ，３７Ｂ，３７Ｃ　第３半導体チップの斜め貫通電極

３８　第３半導体チップの垂直貫通電極

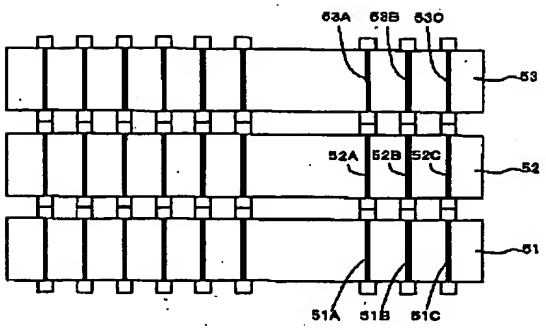
【図１】



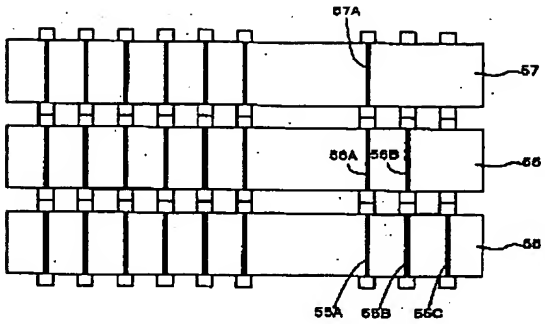
【図２】



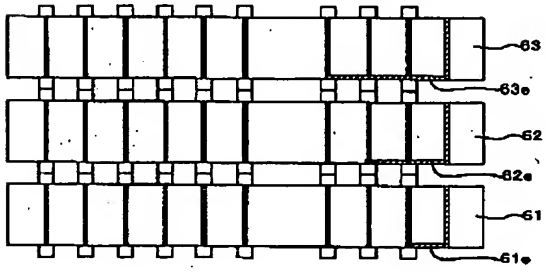
【図３】


53A
53B
53C
53
52A
52B
52C
52
51
51A
51B
51C

【図４】


57A
57
56A
56B
56
55
55A
55B
55C

【図５】


63
63e
62
62e
61
61e